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Title: PREDICTING DEFECT FUTURE EFFECTS IN INTEGRATED CIRCUIT TECHNOLOGY DEVELOPMENT TO FACILITATE SEMICONDUCTOR WAFER LOT DISPOSITION

Inventor: Paul J. Steffan

Docket No.: H0897 Contact: Mikio Ishimaru

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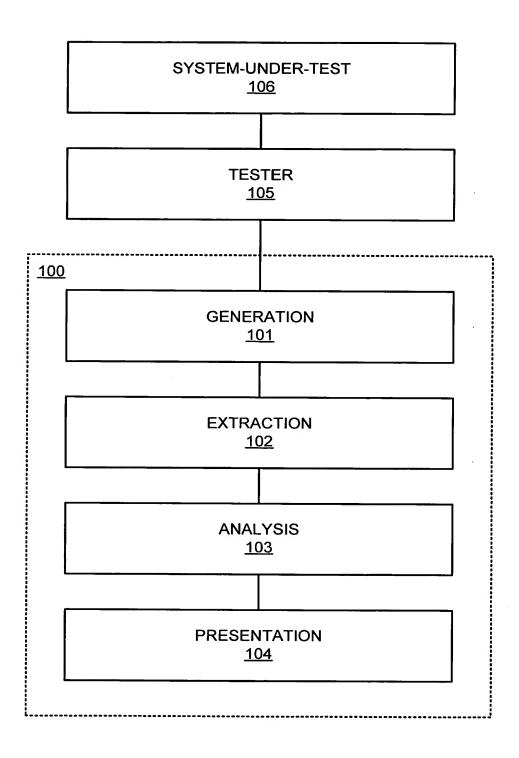


FIG. 1

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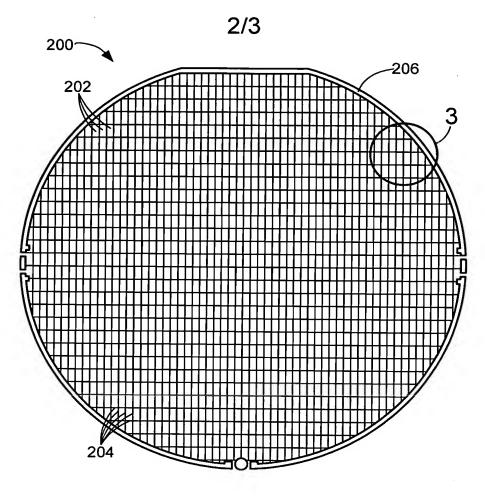
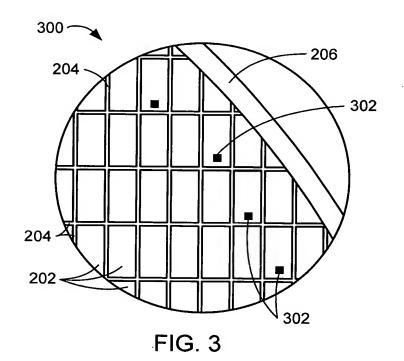


FIG. 2



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Title: PREDICTING DEFECT FUTURE EFFECTS IN INTEGRATED CIRCUIT TECHNOLOGY DEVELOPMENT TO FACILITATE SEMICONDUCTOR WAFER LOT DISPOSITION Inventor: Paul J. Steffan
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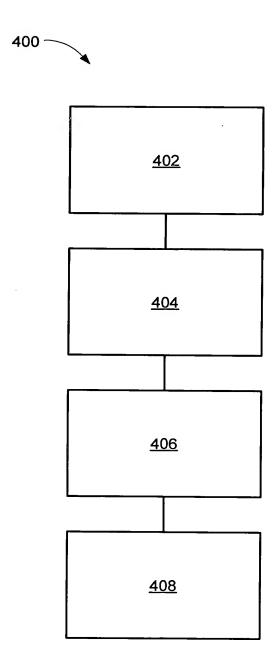


FIG. 4